Abstract

[0054] The tristateless bus interface communication scheme according to the present invention addresses many of the shortcomings of the prior art. In accordance with various aspects of the present invention, a low power embedded system bus architecture is provided with a bus interface connected to one or more peripheral interface using logic processes to enable microcontroller-based products and other components and devices to achieve a low power data transmission between central processors and peripheral devices. In accordance with an exemplary embodiment, a low power embedded system bus architecture comprises logic devices, for example, an OR gate for passing through only data from a selected peripheral device. To facilitate the throughput of data, the non-selected peripheral devices may only provide logic zero to the OR gate. The logic device arrangement may comprise any combination of logic devices which performs the function of eliminating the need for tristate buffers. Through the elimination of tristate buffers, the present invention can lower the power consumed by the microcontroller, and improves the ability to test a large portion of the devices. In accordance with an exemplary embodiment, an AND gate is provided in each peripheral device for providing a logic zero when the peripheral device is not selected, and for providing data when the peripheral device is selected. In addition the AND gate eliminates the occurrence of high impedance Z states.